# Lesson Plan

*Cover Page*: Course Overview

*Semester:* **III**  Year: **2017-18**

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| *Course Title*:  **LOGC DESIGN** | *Course Code*: **16CS35** |
| *Total Contact Hours*: 36 hrs | *Duration of SEE*: 3 **hrs** |
| *SEE Marks*: **100 + 50** | *CIE Marks*: **100** |
| *Lesson Plan Author*: Prof.Prapulla S B, Prof.Kowcika, Dr. Swarnalatha K S, Prof. Chaitra B H | *Date*: **Aug 01, 2017** |
| *Checked By:* | *Date*: 30.6.2017 |

## Course Overview:

This course helps the students to understand the innards of computers. This course deals with the basics of digital logic which includes zeros and ones, representation of signals as a sequence of zeros and ones. Eventually the students will know how large arrays of zeroes and ones can be used in computer files to store information in terms of pictures, documents, audio, and video and how information is transmitted between computers and digital signal sources.

## Course Learning Objectives-CLO

Logic design is a foundation for digital computers, which facilitates the design of electronic circuits, computing, robotics and other electronic applications. Logic design is used to develop hardware such as circuit boards and microchip processors which takes the user input and processes data in computers, navigational systems, cellphones and other electronic systems.

This course lays down the following objectives -

1. To Read and Write Boolean equations for logic circuits.
2. Optimize the Boolean logic expressions.
3. To Design Combinational and Sequential Logical circuits using MSI components.
4. Simulate and experimentally validate Sequential logic circuits.

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| |  |  | | --- | --- | | **Course Outcomes: After completing the course, the students will be able to** | | | 1. | Understand and explore the basic concepts of logic families, Boolean algebra, combinational and sequential circuits. | | 2. | Apply the concepts of simplification to realize the digital circuits. | | 3. | Analyze and evaluate different techniques to realize the digital circuits. | | 4. | Design and develop digital circuits for various applications. | |

**Course Content**

**Course Code: 16CS34**

**Hrs/Week L-T-P-S: 3-0-1-1 CIE: 100 marks**

**Teaching Hours: 36 Hrs PART A SEE: 100 marks**

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|  | **UNIT-I** | **Hours** |
| **1** | **Simplification of Boolean Expressions:**  Karnaughs Map- Using Karnaugh Maps to obtain minimal Expressions for Complete Boolean functions, Minimal Expressions of Incomplete Boolean Expressions, The Quine MC-Cluskey Method of Generating Prime implicants and Prime implicates Prime-Implicant / Prime-Implicate, VEM Technique (up to 4 variables). | **5 Hrs** |
| **2.** | **Logic Families:**  Transistor Transistor Logic (TTL), Static and dynamic hazards in logic circuits | **3 Hrs** |
|  | **UNIT-II** |  |
| **3.** | **Logic Design with MSI Components and Programmable Logic Devices(PLD’s):**  Binary Adders, Substractors, Parallel Adders and Decimal Adders, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices. | **8 Hrs** |
|  | **UNIT-III** |  |
| **4.** | **Flip-Flops and Applications:**  The Basic Bistable Elements, Latches, Timing Considerations, Master-Slave Flip-Flops (Pulse-triggerred Flip-Flops), Edge – Triggerred Flip-Flops, Characteristics Equations, Registers- SISO,SIPO,PISO,PIPO and Universal Shift Register. | **6 Hours** |
|  | **UNIT-IV** |  |
| **5.** | **Counters:**  Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous and Asynchronous Counters. | **5 Hours** |
|  | **UNIT-V** |  |
| **6.** | **Synchronous Sequential Networks:**  Structure and operation of Clocked synchronous Sequential Networks, Analysis of Clocked Synchronous Sequential Networks, Modelling clocked synchronous sequential network behaviour, State Table Reduction, The State Assignment, Completing the design of clocked synchronous sequential networks | **8 Hours** |

**REFERENCE BOOKS:**

1. Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill, 2003 ISBN-13: 0-07-252503-7.
2. Donald P Leach, Malvoni, Gautam Saha “Digital Principles and Applications “, Tata McGraw Hill, 7th Edition 2010.
3. Stephen Brown, “Fundamentals of Digital Logic Design with Verilog”, Tata McGraw Hill, 2nd Edition, 2008.
4. Morris Mano, “Digital Design”, Pearson, Fourth edition, 2006, ISBN-13: 978-0131989245.

**Part B- LAB COMPONENT**

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| **Ex. No.** | **Part A** |
| 1A.    B. | Realization of Excess-3 Code converter with Parallel Adder and Subractor using IC – 7483.  Realization of Binary to Gray Code Converter and vice-versa using IC 74139. |
| 2. | Realization of Full Adder and Full Subtractor using IC 74153. |
| 3. | Design and realization One Bit and Two Bit Magnitude Comparator using Basic Gates. |
| 4A.  B. | Realization of Decoder using IC – 7447.  Realization of Encoder using IC – 74147. |
| 5. | Design and Realization of Master-Slave JK Flip Flop using NAND Gates only. |
| 6 A.  B. | Realization of Up-Down programmable counter using IC 74192 and IC 74193.  Realization of decade counter and its variations using IC 7490. |
| 7 A.  B. | Realization of Ring counter and Johnson counter using IC 7495.  Design and realization of sequence generator using IC 7495. |
| 8. | Design of Mod-N Asynchronous Up and Down counter using IC 7476. |
| 9. | Design of Mod-N Synchronous Up counter using IC 7476. |

**Part B-HDL (Verilog) programs using ModelSim**

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| 1. Write a Verilog code for 8:1 multiplexer, simulate and verify it’s working. |
| 1. Write a Verilog code for a 4 bit comparator using logic gates, simulate and verify it’s working. |
| 1. A. Write a Verilog for D Flip-Flop with positive-edge triggering, simulate and verify it’s working. |
| B. Write a Verilog code for a mod-8 up counter, simulate and verify it’s working. |
| 1. Write a Verilog code for Mod-N Synchronous up-counter. Simulate and verify its truth table. |
| 1. Write the Verilog description code for the given mealy model. |

**Unit and Chapter wise Plan**

**Unit 1**

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*:1. Simplification of Boolean Expressions: | *Planned Hours: 6* **hrs** |

## Learning Objectives:

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| **Sl. No.** | **Objectives** |
| **1** | Demonstrate the knowledge of operation of logic gates (AND, OR, NAND, NOR, XOR). |
| **2** | Draw Boolean Equations for Logic circuits. |
| **3** | Realization of logic circuits for the Boolean expressions using different approaches (Karnaugh simplification, Product-of-sum, Sum-of-products, and Quine-McClusky method). |
| **4** | VEM technique |

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| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. The Basic Gates (NOT, OR, AND) and Universal Gates (NAND, NOR) 2. Boolean Laws and Theorems 3. Sum-of–products method of simplification 4. Truth Table of Karnaugh map 5. Karnaugh map and its simplification techniques 6. Product-of-sum method of simplification 7. Quine-McClusky method of simplification & VEM tyechnique |

## Model Questions

1. State DeMorgan’s First and Second theorem.
2. Draw the logic circuit whose Boolean Equation is Y= (A+B)’ + C.
3. Write a Boolean Expression for an OR gate having A and B as inputs and Y as an Output.
4. Explain the universality of NAND gate.
5. What is the purpose of using an expander with an AND-OR-INVERT gate?
6. What is negative logic?
7. Simplify the following Boolean function using Karnaugh Map in SOP

and POS form: f(A,B,C,D)=∏M(0,3,4,11,13)+dc(2,6,8,9,10)

1. Express the following Boolean function F=AB+A’C in POS form
2. Using Quine Mc-cluskey method, determine all the prime implicants for the

following function: f(v,w,x,y,z)=Σm(4,5,6,7,9,10,14)

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*: *2****.***  Logic Families | *Planned Hours:* ***03*  hrs** |

## Learning Objectives

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| **Sl. No.** | **Objectives** |
| **1** | Different logic families and their comparison |
| **2** | Explain the operation of TTL logic gates ( NAND, NOR and NOT). |
| **3** | Understand the Static and dynamic hazards in logic circuits |

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| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. Transistor – Transistor Logic (TTL), 2. Static and dynamic hazards in logic circuits |

**Model Questions**

1. Discuss the Logic Levels and Noise Margins of LS-TTL
2. Define Fan-in and Fan-out of any logic gate circuit
3. Point out important design concept for a switch using an NPN transistor.

**Unit II**

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*: *3* Logic Design with MSI Components and Programmable Logic Devices(PLD’s) | *Planned Hours:* ***08* hrs** |

## Learning Objectives

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| **Sl. No.** | **Objectives** |
| **1** | Design various Data processing circuits which include Multiplexers, De-multiplexers, 1-of-6 Decoder, Encoders, Ex-OR gates, Magnitude Comparator, Parity Generators, and Checkers. |
| **2** | Demonstrate the organization of Read-only-Memory, programmable array logic and Programmable Logic |
| **3** | Implement Adders and Subtractors using logic gates. |

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| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. Explain decimal adders and Parallel Adder 2. Multiplexers and De-Multiplexers. 3. Decoders and encoders 4. Prority encoders Parity Generators and Checkers 5. Magnitude comparator 6. 1 bit/2 bit/ 4 bit/ nbit comparator 7. Programmable Array Logic (PAL) and Programmable Logic Array (PLA) 8. PROM |

**Model Questions**

* + - 1. Explain the working of 4.bit Carry Look Ahead Adder and Decimal Adder.
      2. Realize a 4 – variable truth table using 8:1 multiplexer for the equation given below Y=F(A,B,C,D)= ∑m(0,2,3,4,5,8,9,10,11,12,13,15)
      3. Describe Prority encoder with a neat block diagram
      4. Design a16 to 1 De-Multiplexer using 4 to 1 multiplexers.
      5. Describe and the principle of operation of PROM, PLA and PAL.

**Unit III**

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*:4. Flip-Flops and Applications | *Planned Hours:* ***07* hrs** |

## Learning Objectives

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| **Sl. No.** | | **Objectives** | |
| **1** | | Describe Characteristic Equations of Flip-Flops and analyze the techniques of Sequential Circuits. | |
| **2** | | Draw and describe the operation of the basic RS-Flip-Flops, Edge Triggered Flip-Flop, D-Flip-Flops, JK-Flip-Flops and Master-Slave JK Flip-Flops. | |
| **3** | | State the cause of Contact Bounce and describe a solution for this problem. | |
| **4** | | Types of Registers | |
| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. Different types of Flip-flops used in Digital systems 2. Switch Contact Bounce Circuits 3. Various representations of flip flops 4. Conversion of flip-flops 5. Edge triggerd flip flops, chracterstic eqations of flip flops 6. Types of registers 7. Universal Shift Register | |

**Model Questions**

1. Draw a circuit for a clocked SR latch and explain its operation
2. Draw the logic circuits for
   * + 1. Master-slave D-flip flop
       2. Edge-Triggered D-flip flop and explain their operations.

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1. Convert JK flip flop to D flip flop.
2. Derive the characteristics equation of JK Flip flop.
3. Explain the working of Master Slave JK flip flop. Draw its timing diagram.
4. Using logic circuit, truth table and timing diagram, explain the operation of SR flip flop. Show the excitation table and characteristics equations.
5. What are the different types of registers? Explain any two of them.
6. What is a shift register? Explain different types of shift registers.
7. . Explain briefly two applications of shift registers.
8. . Draw the block diagram of a 4 bit binary ripple counter using JK flip flops and explain its working. Also draw the timing diagram.

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## UNIT- IV

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*: *5****.***   Counters | *Planned Hours: 0****6* hrs** |

## Learning Objectives

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| **Sl. No.** | **Objectives** |
| **1** | **Asynchronous Counters** |
| **2** | Synchronous Counters |
| **3** | Changing the modulous |

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| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. Design of Asynchronous Counters 2. Design of Synchronous Counters 3. Analysis of Synchronous Counters |

**Model Questions**

1. Describe the basic construction and operation of Asynchronous and Synchronous Counters.
2. Design Modulo-N-Synchronous and Asynchronous Counters.
3. Design a self-correcting mod-6 counter in which all the unused state leads to state

**Unit V**

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| *Course Code and Title:* (**16CS34) Logic Design** | |
| *Chapter Number and Title*: 6. Synchronous Sequential Networks | *Planned Hours:* ***06* hrs** |

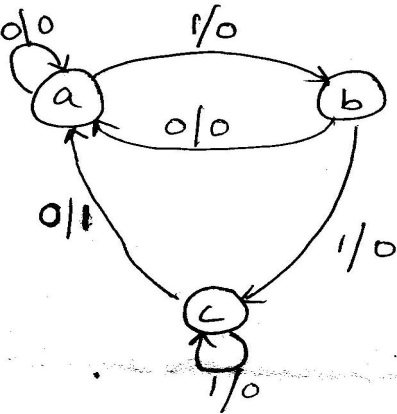
## Learning Objectives

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| **Sl. No.** | **Objectives** |
| **1** | State Transition Diagram and the preparation of State Synthesis table. |
| **2** | Describe the design issues related to Asynchronous Sequential Circuits. |
| **3** | State Machine Design using Moore model and Mealy model |
| **4** | Implement Sequential Circuits using Read-only-Memory. |
| **5** | State Reduction Techniques. |

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| ***Lesson Schedule***  *Class No. Portion covered per hour*   1. Design and Implementation of Sequential Circuits, equations and Circuit diagram 2. Algorithmic state design and the sate reduction technique 3. Analysis and the Design of Asynchronous Sequential circuit and the problems with it. 4. State table reduction 5. Clocked synchronous sequential networks. |

**Model Questions**

1. With the help of neat diagram explain Moore model and Mealy model of a clocked synchronous sequential network.
2. 2. Discuss how excitation tables, state tables and state diagrams are used to analyze a synchronous sequential network.
3. Design a circuit diagram for the following state transition diagram using Mealy model:



**LESSON PLAN /WEEK**

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| **Week** | **Day** | **Unit** | **Main topic** | **Sub topic** | **No. Hr** | **ICT tools Used** | **Book Referred** |
|  | 1 | I | Simplification of Boolean Expressions | Karnaughs Map- Using Karnaugh Maps to obtain minimal Expressions for Complete Boolean functions | 01 | Lecture(Black Board)+ TPS | Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill, 2003 ISBN-13: 0-07-252503-7 |
| 2 | Minimal Expressions of Incomplete Boolean Expressions | 01 | Flipped Classroom with TPS |
| 3 | The Quine MC-Cluskey Method of Generating Prime implicants and Prime implicates Prime-Implicant / Prime-Implicate | 02 | Flipped Classroom with TPS |
| 4 | VEM Technique (up to 4 variables). | 01 | Lecture(Black Board) + Problem Solving |
|  | 5 |  | Logic Families | Transistor Transistor Logic (TTL) | 02 | Lecture(Black Board) | Donald P Leach,0020Malvoni, Gautam Saha “Digital Principles and Applications “, Tata McGraw Hill, 7th Edition 2010 |
| 6 | Static and dynamic hazards in logic circuits | 01 | Lecture(Black Board) |
|  | 9 | II | Logic Design with MSI Components and Programmable Logic Devices(PLD’s) | Binary Adders, Substractors | 01 | Lecture(Black Board) | Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill, 2003 ISBN-13: 0-07-252503-7 |
| 10 | Parallel Adders and Decimal Adders | 01 | Lecture(Black Board) |
| 11 | Comparators | 01 | Lecture(Black Board) |
| 12 | Decoders | 02 | Lecture(Black Board) + Problem Solving |
| 13 | Encoders | 01 | Flipped Class Room with TPS |
| 14 | Multiplexers | 01 | Lecture (Black Board) + TPS |
| 15 | Programmable Logic Devices | 01 | Lecture(Black Board) + Problem Solving |
|  | 13 | III | Flip-Flops and Applications | The Basic Bistable Elements, Latches | 01 | Power Point Presentation |
| 14 | Timing Considerations | 01 | Power Point Presentation |
| 15 | Master-Slave Flip-Flops (Pulse-triggerred Flip-Flops) | 01 | Lecture + Power Point Presentation |
| 16 | Edge – Triggerred Flip-Flop Characteristics Equations | 01 | Lecture(Black Board) |
| 18 | Registers- SISO,SIPO,PISO,PIPO | 01 | Lecture(Black Board) + Power Point Presentation |
| 19 | Universal Shift Register | 01 | Lecture(Black Board) + Power Point Presentation |
|  | 20 | IV | Counters | Binary Ripple Counters | 01  Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill, 2003 ISBN-13: 0-07-252503-7 | Lecture (PPT, Black Board) |
| 21 | Synchronous Binary Counters | 01 | Lecture (PPT, Black Board) |
| 22 | Counters based on Shift Registers | 01 | Lecture (PPT, Black Board) |
| 23 | Design of Synchronous and Asynchronous Counters | 02 | Flipped Class room with Team pair solo |
|  | 24 | V | Synchronous Sequential Networks | Structure and operation of Clocked synchronous Sequential Networks | 01 | Lecture (PPT, Black Board) |
| 25 | Analysis of Clocked Synchronous Sequential Networks | 01 | Lecture (PPT, Black Board) + Problem Solving | Donald D.Givone, “Digital Principles and Design”, Tata McGraw-Hill, 2003 ISBN-13: 0-07-252503-7 |
| 26 | Modeling clocked synchronous sequential network behavior | 02 | Lecture (PPT, Black Board) + Problem Solvings |
|  | 27 | State Table Reduction, The State Assignment | 02 | Lecture + TPS |
| 28 | Completing the design of clocked synchronous sequential networks | 02 | Lecture (PPT, Black Board) + Problem Solving |

# Evaluation Scheme

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| **Continuous Internal Evaluation (CIE)**  **( Theory – 100 Marks)** | |
| Evaluation method | Course with Self-study |
| Quiz -1 | 10 |
| Test -1 | 25 |
| Quiz -2 | 10 |
| Quiz -3 | 10 |
| Test -2 | 25 |
| EL | 20 |
| LAB | 50 |
| **Total** | **150** |

**Experiential Learning**

**The course has experiential learning as one of the assessment tool. In this regard Open Ended Experiments will be introduced as a part of Experiential Learning. Open ended experiments could be Hardware/Matlab/Xilinx/Simulink/ModelSim implementations with results. Implementation of a digital system of their choice which is different from those taught in the class. It has to be a working project implemented on Matlab/Xilinx/Simulink/ModelSim/Hardware. The details of the project should be well documented.**

**Sample Experiments List**

1. **HDL models of data storage elements**
2. **12h/24h Digital Clock Circuit Design using Counters**
3. **Traffic Sensors using logic gates**
4. **One-way Road Intersection Traffic Light**
5. **LED Chandelier**
6. **RGB LED Bulb**
7. **Boolean Algebra Calculator**
8. **Metal Detector Circuit**
9. **JK Flip Flop using CD4027**
10. **Police Lights using 555 Timer**

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| **Components** | **Rubrics for Experiential Learning (Hardware/Simulation)** | | |
|  | **Excellent** | **Good** | **Not Satisfactory** |
| **Objective (2)** | Clearly State the objective of the experiment in your own words.  (2-1.5 marks) | Somewhat clear in stating the objective of the experiment.  (1 mark) | Not Clear about the Experiment-  (0 Marks) |
| **Design(6)** | Clearly State the Design Requirements with circuit implementation consisting of minimum hardware.  (6-4 marks) | Somewhat clear in Design requirements and the circuit implementation.  (1-3 Marks) | Not implemented-  (0 marks) |
| **Hardware or Simulation(4)** | Complete information of hardware equipment with the components.  (4-3marks) | Little information of hardware equipment and its components  (1-2 marks) | Not clear about the hardware.  (0 marks) |
| **Demonstration (4)** | Explain the working of the circuit along with its applications.  (4-3marks) | Explain the working of the circuit but not clear with its applications.  (1-2 marks) | Not clear with the working of the circuit.  (0 marks) |
| **Analysis (4)** | Circuit Performance is measured and is very good.  (4-3marks) | Circuit performance is good.  (1-2 marks) | Circuit performance not measured.  (0 marks) |

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**Digital Logic Design Lab Rubrics (16CS34)**

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|  |  | | **Excellent** | | **Good** | **Poor** |
| a. | **Knowledge / Understanding**  **(2 Marks)** | | Demonstrates thorough ability in describing and illustrating the function of the circuit (2-1.5) | | Demonstrates considerable ability in describing and illustrating the function of the circuit (1-0.5) | Unable to demonstrate, describe and illustrate the function of the Circuit (0) |
| b. | **Circuit Construction**  **(2 Marks)** | | Excellent circuit functional, construction (2-1.5) | | Fair circuit functional, construction (1-0.5) | Poor circuit functional, construction (0) |
| c. | **Circuit Data Recording**  **(2 Marks)** | | Correct data input and excellent presentation (2-1.5) | | Correct data input and fair presentation (1-0.5) | Correct data input and poor presentation (0) |
| **Viva rubrics (Max: 4 marks)** | | | | | | |
|  | |  | | **Excellent** | **Good** | **Poor** |
| a. | | **Circuit Data Analysis**  **(2 Marks)** | | Answers to data analysis questions, show complete understanding of how the circuit works (2-1.5) | Answers to data analysis questions, show solid understanding of how the circuit works (1) | Answers to data analysis questions, show no understanding of how the circuit works (0) |
| b. | | **Applications**  **(1 Mark)** | | Demonstrates a high ability when wiring logic gates to construct logical circuits (1) | Demonstrates considerable ability when wiring logic gates to construct logical circuits(0.5) | Demonstrates very limited ability when wiring logic gates to construct logic circuits (0) |
| c. | | **Communication of Ideas**  **(1 Mark)** | | Communicates all ideas clearly (1) | Communicates limited ideas (0.5) | Unable to communicate ideas(0) |

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| **Semester End Evaluation Theory (150)** | |
| **Part- –A**  **Objective type questions** | **20** |
| **Part –B**  There should be five questions from five units. Each question should be for maximum of 16 Marks.  The **UNIT-1**, **UNIT-4** and **UNIT-5** should not have any choice.  The **UNIT-2 and UNIT-3** should have an internal choice.  Both the questions should be of the same complexity in terms of COs and Bloom’s taxonomy level. | **80** |
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| **LAB** | **50** |
| **Total** | **150** |

## Course Unitization for Internals and Semester End Examination

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| **Part** | **Chapter** | | **Teaching Hours** | **No. of Questions in** | | **No. of Questions in SEE** |
| **Internals I** | **Internals II** |
| **Unit 1** | 1 | **Simplification of Boolean Expressions** | 6 | 1 | -- | 1 |
| 2 | **Logic Families** | 3 | 1 | -- |
| **Unit 2** | 3 | **Logic Design with MSI Components and Programmable Logic Devices(PLD’s)** | 8 | 1 | -- | 1 |
| **Unit 3** | 4 | **Flip-Flops and Applications** | 7 | -- | 1 | 1 |
| **Unit 4** | 5 | **Counters** | 6 | -- | 1 | 1 |
| **Unit 5** | 6 | **Synchronous Sequential Networks** | 6 | -- | 1 | 1 |

**Faculties In-charge Head of Department**

**Course Articulation Matrix (16CS34)**

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| |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **CO-PO Mapping** | | | | | | | | | | | | | | | **CO/PO** | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | | **CO1** | L | L | - | - | L | - | L | - | - | - | - | L | | **CO2** | M | M | - | - | L | - | L | - | M | M | - | L | | **CO3** | M | - | L | - | L | - | L | - | M | M | - | L | | **CO4** | - | L | M | - | L | - | M | - | M | L | - | L | |

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| **Program Articulation Matrix**   |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Course - PO Mapping** | | | | | | | | | | | | | | |  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | | **Course** | **L** | **L** | **L** | **-** | **L** | **-** | **L** | **-** | **M** | **L** | **-** | **L** | |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **CO –PSO Mapping** | | |  | **Course – PSO Mapping** | | | | **CO/PSO** | **PSO1** | **PSO2** |  | **Course** | **PSO1** | **PSO2** | | **CO1** | **-** | **-** |  | **M** | **L** | | **CO2** | **L** | **-** |  |  |  |  | | **CO3** | **M** | **L** |  |  |  |  | | **CO4** | **H** | **L** |  |  |  |  |   **CO-PSO Mapping COURSE-PSO Mapping** |

**Flipped Class Room Activity**

**Out\_of\_class Activity Design-1:**

Uploaded Video URL: <https://youtu.be/hKILyBAIeHE>

License of Video: Creative common attribution License

Duration of video: V1-6 MIN

**After watching the video student should be able to know**

1. **Minimize the incomplete Boolean expressions using Karnaugh maps.**
2. **Represent Boolean expressions in SOP and POS form.**
3. **Design the circuits using logic gates.**

**Key Concept(s) to be covered:**

1. Karnaugh Maps
2. Don’t Care conditions

**Out-of-class Activity Design – 2**

Uploaded Video URL: <https://youtu.be/4yenaTimgGM>

License of Video: Creative common attribution License

Duration of video: V1-10.04 MIN

**After watching the video student should be able to know**

1. **Minimize thecomplete/incomplete Boolean expressions using QM (Tabular) Method.**
2. **Represent Boolean expressions in SOP and POS form.**
3. **Design the circuits using logic gates.**

**Out-of-class Activity Design – 3**

Uploaded Video URL: https: <https://youtu.be/kEj-m3YuGa4>

**Published on 23 Jan 2015**

Digital Electronics: Priority Encoder  
  
Contribute: <http://www.nesoacademy.org/donate>

Duration of video: V1-10.49 MIN

**After watching the video student should be able to know**

* 1. **About Encoders**
  2. **How they are different from Decoders**
  3. **Advantages of Priority Encoder**

**Out-of-class Activity Design – 4**

Uploaded Video URL: https:/<https://youtu.be/dafdMP6d7GY>

License of Video: Creative common attribution License

Duration of video: V1-6.37 MIN

**After watching the video student should be able to know**

1. **The function table of SR flip flop and D Flip Flop.**
2. **The K-map simplification representing the characteristic expressions for the same.**

**Think-Pair-Share (TPS) Activity:**

Domain: Logic Design

Topic: Using Karnaugh Maps to obtain minimal Expressions for Complete Boolean functions

Target Students: BE (CSE) 3rd Sem

Think Phase -              [3 minutes]

Question:

**Reduce the following function using K-Map and implement the resulting function using basic gates.**

1. **f(p, q, r, s) = ∑m(0,1,2,4,8,9,10)**
2. **f(w, x, y, z) = πM(0,2,4,10,11,14,15)**

What Teacher does - Poses the question, asks students to think individually and write the minimized SOP/POS expression

What students do - **Thinks individually and Write down minimized SOP/POSexpressions.**

Pair Phase -                [7 minutes]

Question: Discuss your answer with your neighbors and verify if any terms are extra (repeated).

What Teacher does - Poses the question, asks students to pair up and discuss, goes around the class to check whether students are discussing, and provides clues to pairs who are in doubt.

What students does - Pairs up with neighbors, Checks each other’s result.

Share Phase -              [5 minutes]

What Student Does – Shares the result with whole class.

What Teacher Does - **Notes down the correct answer in the board, summarizes the key concepts involved in this problem.**

**Flipped Class Room Activity Incharges:**

|  |  |  |
| --- | --- | --- |
| **Sl No** | **Topic** | **Faculty** |
| 1 | Characteristic Equations of Flip Flops | CBH |
| 2 | Karnaugh Map Simplification for incomplete Boolean Functions+ QM Method | PSB |
| 3 | Asynchronous and Synchronous Counters | KA |
| 4 | Priority Encoders | SL |